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(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
31 October 2002 (31.10.2002)

PCT

(10) International Publication Number
WO 02/086686 A1

(51) International Patent Classification[7]: G06F 1/04

(21) International Application Number: PCT/GB02/01324

(22) International Filing Date: 21 March 2002 (21.03.2002)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
0110059.3 24 April 2001 (24.04.2001) GB

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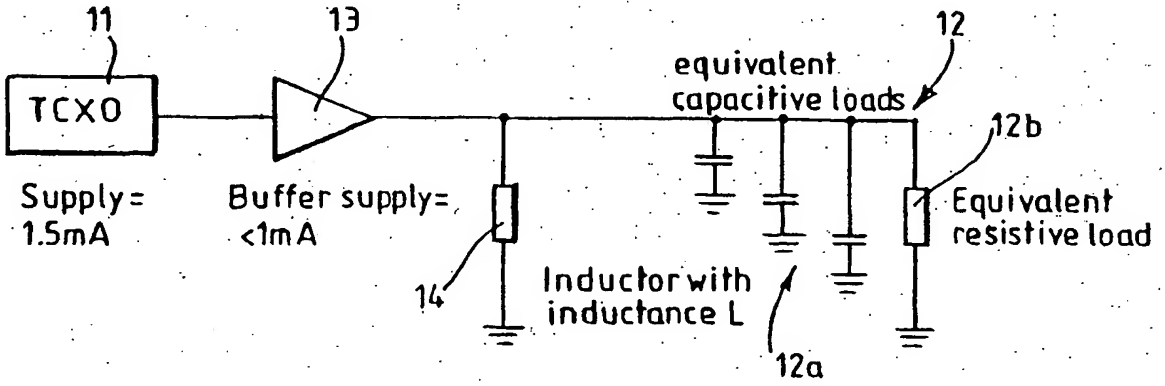
(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, OM, PH, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZM, ZW.

(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: CLOCK DISTRIBUTION CIRCUIT



(57) Abstract: A clock distribution circuit is disclosed for a battery-powered device such as a mobile telephone or a PDA. The clock distribution circuit comprises an oscillator (11), a load (12), and a buffer amplifier (13) between the oscillator and the load. The load (12) includes a resistance and a capacative reactance. An inductor (14) is positioned between the buffer amplifier (13) and the load (12), the inductor being rated so as to resonate with the capacative reactance of the load.

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Clock Distribution Circuit

This invention relates to a clock distribution circuit, and in particular to a clock distribution circuit for use with a battery-powered device such as a mobile telephone handset or a personal digital assistant (PDA).

The various operations of a device such as a mobile telephone handset are controlled using a reference clock that generates periodic signals that are used to synchronise these operations. A typical mobile telephone handset will contain a clock circuit of the type shown in Figure 1, in which a temperature compensated crystal oscillator (TCXO) 1 provides a reference clock. The reference clock 1 is routed to a number of different circuits, indicated generally by the reference numeral 2 within the handset, these circuits typically including RF frequency synthesisers and a baseband digital processor. The sum of the loads presented by these circuits can be considered as capacitances 2a in parallel with a resistance 2b as indicated schematically in Figure 1. The resistance 2b is typically high (in the range of from 1 kOhm to 10 kOhm, and very little current is required to develop a voltage across it. However, the capacitance 2a appears as a load reactance of ~ - 352 jOhm. The capacitance associated with the inputs to the different integrated circuits within the handset and with the clock distribution tracking, a total of typically 35 pF, would be an excessive load for the oscillator 1, which is typically specified for use with a load of approximately 2 pF. A buffer amplifier 3 is, therefore, positioned between the oscillator 1 and the integrated circuits 2 to provide higher drive capability. In a typical arrangement, the buffer amplifier 3 is arranged to provide a signal level of 0.8 volt peak-peak into the load at a frequency of 13 MHz. The peak current (I) in the load can be calculated from the formula

$$I = \frac{V}{R} \cdot \sqrt{1 + 4\pi^2 f^2 Ct^2 R^2}$$

where V is the peak voltage, R is the total load resistance, and Ct is the total load capacitance, and is 1.16 mA for a load capacitance of 35 pF, a load resistance of 2000 Ohm and a peak-to-peak load voltage of 0.8 volts. In addition, a load waveform with symmetrical positive and negative half cycles is typically required, which requires that the buffer amplifier 3 must be operated in a linear mode. For linear operation, however,

a bias current of between two and three times the load current is required. In a typical mobile 'phone handset, the oscillator and clock distribution will always be powered when the handset is switched on. Consequently, current drawn by the oscillator 1 and the buffer amplifier 3 will reduce the standby time of such a handset.

The aim of the invention is to provide a clock distribution circuit for a mobile 'phone handset which has a reduced current consumption, and hence an increased standby time.

The present invention provides a clock distribution circuit for a battery-powered device, the clock distribution circuit comprising an oscillator, a load, and a buffer amplifier between the oscillator and the load, the load comprising a resistance and a capacitive reactance, wherein an inductor is positioned between the buffer amplifier and the load, the inductor being rated so as to resonate with the capacitive reactance of the load.

In a preferred embodiment, the inductor is in parallel with the load. In this case, the circuit may further comprise a resistor in parallel with the inductor

Alternatively, the inductor is in series with the buffer amplifier. In this case, the circuit may further comprise a resistor in series with the inductor.

Preferably, the inductor has a rating L given by the formula

$$L = \frac{1}{4\pi^2 f^2 Ct}$$

where f is in the frequency of the oscillator, and Ct is the total load capacitance

In a preferred embodiment, the circuit further comprises a capacitor in parallel with the inductor, the arrangement being such that the capacitor and the inductor are parallel resonant at the second harmonic of the clock frequency, and such that the parallel combination of the inductor and the capacitor is series resonant with the load at the clock frequency. This results in a load waveform with a duty cycle close to 50%.

Advantageously, the circuit further comprises a resistor in series with the parallel combination of the inductor and the capacitor.

Conveniently, the inductor has a value L given by the formula

$$L = \frac{3}{16\pi^2 f^2 Ct}$$

and the capacitor has a value C given by the formula

$$C = \frac{Ct}{3}$$

where f is the frequency of the oscillator, and Ct is the total load capacitance.

Where the circuit further comprises a resistor, it may be so rated that the Q factor of the circuit is greater than one, and preferably is between two and five. The resistor reduces the variation of the load voltage for variations in the clock load capacitance and inductor value variation.

The invention will now be described in greater detail, by way of example, with reference to the accompanying drawings, in which:-

Figure 1 is a prior art clock distribution circuit; and

Figure 2 is a first form of clock distribution circuit according to the invention.

Figure 3 is a second form of clock distribution circuit according to the invention;

Figure 4 is a third form of clock distribution circuit according to the invention;

Figure 5 is a diagram of a practical clock distribution circuit equivalent to the circuit of Figure 2; and

Figure 6 is a diagram of a practical clock distribution circuit equivalent to the circuit of Figure 4.

Referring to the drawings, Figure 2 shows a clock distribution circuit having a temperature compensated crystal oscillator (TCXO) 11, and a plurality of different circuits within the handset, these circuits being indicated by the reference numeral 12 and typically including RF frequency synthesisers and a baseband digital processor. The sum of the loads presented by these circuits can be considered as capacitances 12a in parallel with a resistance 12b, as indicated schematically in Figure 2. As with the

prior art circuit, a buffer amplifier 13 is positioned between the oscillator 11 and the load circuit 12. The circuit of the invention does, however, include an inductor 14 in parallel with the buffer amplifier 13 at the output thereof. The value 4.3 μH of the inductor 14 is chosen to resonate with the capacitive reactance of the load (~- 350 jOhm) at a clock frequency of 13 MHz. Energy is stored in the inductor 14 and in the capacitive part 12a of the load, and alternates at the clock frequency between the inductor and the capacitance.

The stored energy accumulates over a number of cycles, such that the total stored energy is greater than the energy supplied from the buffer amplifier 13 during one cycle. The buffer amplifier 13 has to provide enough power every cycle to generate the required load voltage across the equivalent load resistance 12b. The energy supplied from the amplifier 13 can consequently be relatively small compared to the total energy within the clock circuit, allowing the power consumption of the clock buffer circuit to be reduced. It must also be noted that energy storage is most effective at the resonant frequency of the network. At the harmonic frequencies of the oscillator 11, energy storage is minimal, and energy at the harmonic frequencies is attenuated relative to that at the fundamental frequency. Asymmetry of the load voltage waveform can be attributed to the presence of even harmonics of the clock. The attenuation of harmonic energy within the circuit results in a load voltage waveform that is substantially sinusoidal. A further benefit arising from the reduction of clock harmonics is that the possibility of interference to other circuits within the handset, and to external devices, is reduced. Moreover, for the circuit to function advantageously, the output impedance of the buffer amplifier 13 must be high relative to the load impedance at the resonant frequency.

In a perfect circuit, with the inductor 14 tuned to resonate exactly at the clock frequency, the drive amplifier would only need to supply sufficient current to develop the voltage across the resistive part of the load. In practice, variation in the equivalent load capacitance 12a and the inductance 14 due to component tolerance means that it is not possible to ensure the circuit remains resonant exactly at the clock frequency. Variations in the resonant frequency can give rise to excessive variations of load

voltage due to the changing level of energy storage away from resonance. Sensitivity to component variation can be reduced by lowering the quality factor (Q) of the circuit by including additional resistive elements within the circuit. To reduce the Q in the circuit of Figure 2, a resistor (not shown) may be added in parallel with the inductor 14 A disadvantage of including resistive elements is that additional power must be supplied from the buffer amplifier 13. However, providing the Q of the circuit is greater than one, then energy is stored for more than one cycle, and a reduction in total power consumption over the circuit of Figure 1 can be realised. In practice, Q values of between two and five are most advantageous.

Figure 3 shows an alternative form of the circuit of Figure 2, so like reference numerals are used for like parts, and only the modifications will be described in detail. Thus, the main difference between the two circuits is that the inductor 14' of Figure 3 is in series with the buffer amplifier 13 rather than being in parallel. For the circuit to function advantageously, the output impedance of the buffer amplifier must be low relative to the load impedance at the resonant frequency.

To allow for component variation, a series resistor (not shown) may be included in series with the inductor 14', thereby to reduce the Q factor of the circuit. The resistor would allow greater changes in the circuit component values without the drive level to the load varying significantly. One disadvantage of including the series resistor, is that some of the energy from the drive circuit is dissipated. However, as long as the Q factor of the circuit is greater than one, an improvement in total current consumption is realised. In practice, Q values of between two and five are most advantageous.

It will be appreciated that the rating (L) of the inductor 14 (or 14') depends upon factors such as the operating frequency (f) of the oscillator 11, and the total load capacitance (Ct) which is the sum of all the load capacitances 12a. The value L is given by the formula:-

$$L = \frac{1}{4\pi^2 f^2 Ct}$$

For the typical application described above with reference to Figure 4, C_t is 35 pF and the operating (clock) frequency is 13 MHz, giving rise to the quoted values of 4.3 μH for the inductor 14 (or 14').

A further aspect of the invention relates to providing a signal with a 50% duty cycle and a low harmonic content. Waveform asymmetry can be seen to be due to the presence of even harmonics of the clock. In particular, the presence of a second harmonic is usually the greatest source of waveform asymmetry. In order to attenuate the second harmonic current in the load, the circuit of Figure 3 may be modified, as shown in Figure 4, by placing a capacitor 15 (11.7 pF) in parallel with the inductor 14', so that the capacitor and the inductor are parallel resonant at the second harmonic of the clock frequency. Here again, as the circuit of Figure 4 is very similar to that of Figure 3, like reference numerals will be used for like parts, and only the modifications will be described in detail. The parallel combination of the inductor 14' and the capacitor 15 is such that they are series resonant with the load at the clock frequency as described above. The parallel resonance of the LC circuit impedes the flow of the second harmonic current from the buffer amplifier 13 to the load 12, and results in a load voltage waveform that is substantially sinusoidal, with symmetrical positive and negative half cycles. Moreover, the load waveform symmetry is typically improved over that at the output of the oscillator 11. A further benefit arising from the reduction of clock harmonics is the reduction of interference between other circuits within the handset and external devices.

For the circuit of Figure 4, the inductor 14' and the capacitor 15 are rated (L and C respectively) according to the formulae:-

$$L = \frac{3}{16\pi^2 f^2 C_t}$$

$$C = \frac{C_t}{3}$$

As with the earlier embodiments, to allow for component variation, a resistor (not shown) may be included in series with the parallel combination of the inductor 14' and the capacitor 15, thereby to reduce the Q factor of the series resonance of the circuit.

The resistor would allow greater changes in the circuit component values without the drive level to the load varying significantly. One disadvantage of including the series resistor, is that some of the energy from the drive circuit is dissipated. However, as long as the Q factor of the circuit is greater than one, an improvement in total current consumption is realised. In practice, Q values of between two and five are most advantageous.

Diagrams for two practical clock circuits for use in a GSM cellular handset are shown in Figures 5 and 6. The circuit of Figure 5 is a parallel resonant circuit, and is most suitable for use where the output waveform of the oscillator 11 contains a low level of even harmonics. The circuit uses a bipolar transistor Q1 within the buffer amplifier, the base of the transistor being biased by resistors R1 (33 kOhm) and R2 (33 kOhm). Resistors R4 (680 Ohm) and R5 (470 Ohm) are used to set the emitter bias current, and are chosen to set the required level of clock signal at the output. A capacitor C4 (1 nF) decouples the resistor R4 to ground such that the gain of the amplifier at 13 MHz is set by the resistor R5, and the combined resistance of the collector load. The gain is such that the transistor emitter current is zero for a short period during the negative peak of the input waveform. This results in some compression, and a reduction in the output level variation with input level change. However, the degree of compression is insufficient to generate significant levels of unwanted harmonics at the output. Capacitors C1 (100 pF) and C3 (1 nF) are used to isolate the amplifier bias voltages from the source and load, and a capacitor C2 (10 nF) decouples the amplifier power supply to ground such that the power supply appears as a virtual ground at the clock frequency. The inductor 14' (3.9 μH) is chosen to resonate with the equivalent load capacitance at the 13 MHz clock frequency. The Q-factor is limited to approximately three by the resistor R1, the equivalent load resistor 12b (2000 ohm) and additional losses in the inductor 14' and the transistor Q1. The circuit provides an output voltage swing of 800mV peak-to-peak, and consumes 400μA of current from a 2.8V power supply.

The circuit of Figure 6 is a series resonant circuit, and is suitable for use where the output of the oscillator 11 contains a high level of second harmonic. Alternative

arrangements of the amplifier and tuned circuit are possible. However, these all require additional components, and are consequently less advantageous for use in low cost consumer products. Design of the circuit is more complicated than that of Figure 4, and is most easily accomplished with circuit simulator software. The circuit uses a bipolar transistor Q1 within the buffer amplifier, and the base of the transistor is biased by resistors R1 (12 kOhm), R2 (150 kOhm) and R3 (3.3 kOhm), the capacitance 12a (35 pF), the inductor 14' (3.9μH), the capacitors 15 (8.2 pF) and C3 (10 nF), and the emitter of the transistor Q1. A resistor R4 (3.9 kOhm) is used to set the emitter bias current, and is chosen to set the required level of clock signal at the output. Capacitors C1 (100 pF) and C3 (10 nF) are used to isolate the amplifier bias voltages from the source and load, and a capacitor C2 (10 nF) decouples the amplifier power supply to ground such that the power supply appears as a virtual ground at the clock frequency. The amplifier operates in a non-linear mode, with the transistor emitter current at zero for approximately 55% of the clock period. During the period that the transistor emitter current is zero, the resonant circuit current flows predominantly through the capacitance 12a, the capacitor 15, the inductor 14', the capacitor C3 and a capacitor C5 (100 pF). The change in current path causes the resonant frequency to shift slightly during the cycle. The component values are picked such that the average resonant frequency is at 13 MHz. The parallel resonance of the capacitor 15 and the inductor 14' prevents second harmonic currents from flowing in the tuned circuit, and ensures the output voltage waveform is substantially sinusoidal. The Q-factor is determined from the time weighted average of loss for the two different resonant current paths. For the values shown, the Q is approximately four. The circuit provides an output voltage swing of 800mV peak-to-peak, and consumes 500μA of current from a 2.8V power supply.

Claims

1. A clock distribution circuit for a battery-powered device, the clock distribution circuit comprising an oscillator, a load, and a buffer amplifier between the oscillator and the load, the load comprising a resistance and a capacitive reactance, wherein an inductor is positioned between the buffer amplifier and the load, the inductor being rated so as to resonate with the capacitive reactance of the load.

2. A circuit as claimed in claim 1, wherein the inductor is in parallel with the load.

3. A circuit as claimed in claim 2, further comprising a resistor in parallel with the inductor.

4. A circuit as claimed in claim 1, wherein the inductor is in series with the load.

5. A circuit as claimed in claim 4, further comprising a resistor in series with the inductor.

6. A circuit as claimed in claim any one of claims 2 to 5, wherein the inductor has a rating L given by the formula

$$L = \frac{1}{4\pi^2 f^2 Ct}$$

where f is in the frequency of the oscillator, and Ct is the total load capacitance

7. A circuit as claimed in claim 4, further comprising a capacitor in parallel with the inductor, the arrangement being such that the capacitor and the inductor are parallel resonant at the second harmonic of the clock frequency, and such that the parallel combination of the inductor and the capacitor is series resonant with the load at the clock frequency.

8. A circuit as claimed in claim 7, further comprising a resistor in series with the parallel combination of the inductor and the capacitor.

9. A circuit as claimed in claim 7 or claim 8, wherein the inductor has a value L given by the formula

$$L = \frac{3}{16\pi^2 f^2 Ct}$$

where f is the frequency of the oscillator, and Ct is the total load capacitance.

10. A circuit as claimed in claim 9, wherein the capacitor has a value C given by the formula

$$C = \frac{Ct}{3}$$

where Ct is the total load capacitance.

11. A circuit as claimed in claim 3, claim 5 or claim 8, wherein the resistor is so rated that the Q factor of the circuit is greater than one.

12. A circuit as claimed in claim 11, wherein the resistor is such that the Q factor of the circuit is between two and five.

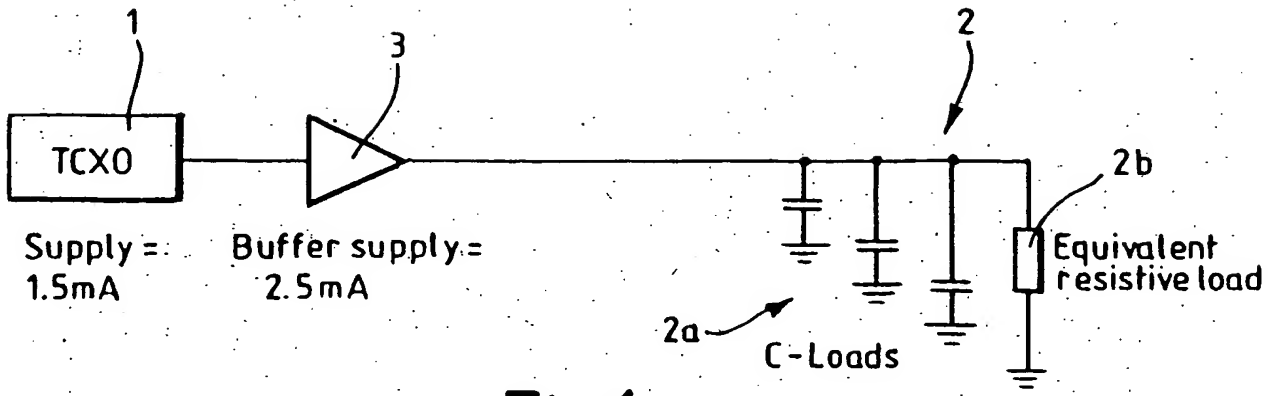

Fig.1.

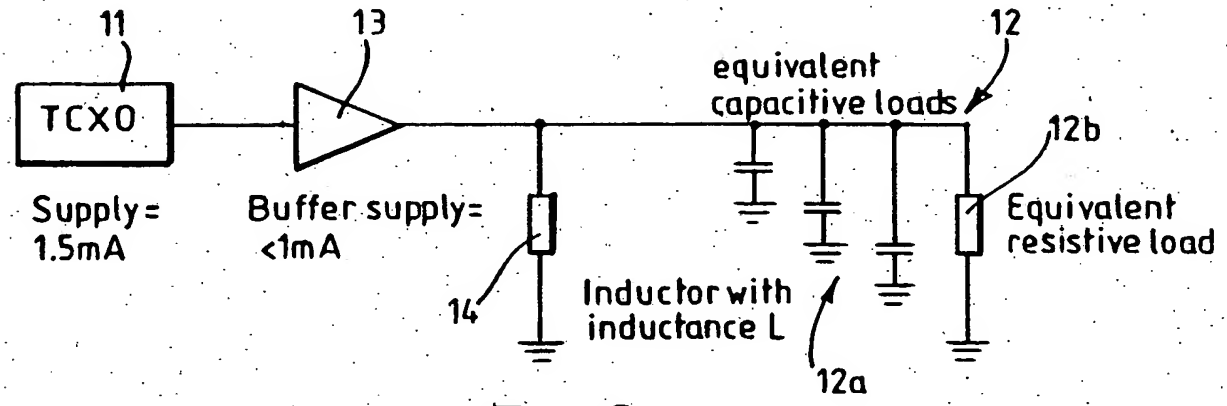

Fig.2.

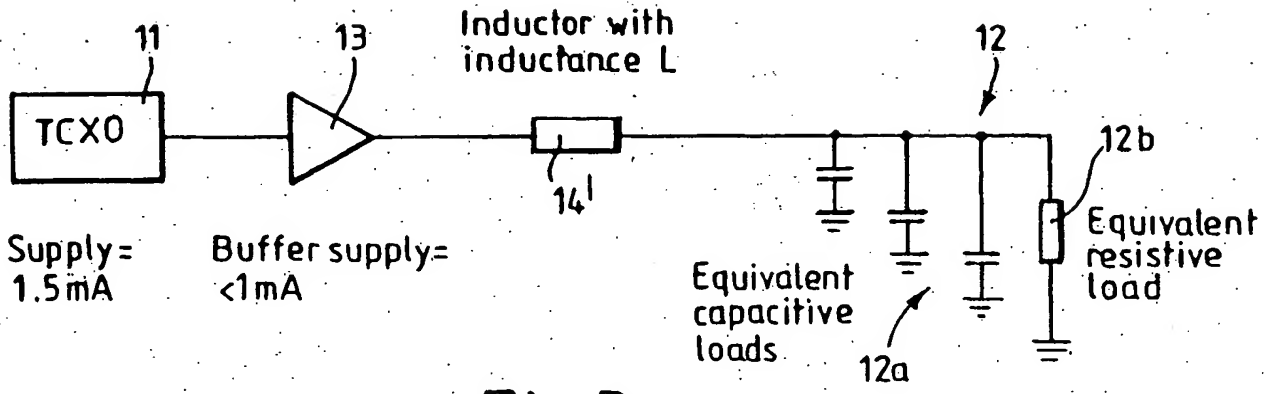

Fig.3.

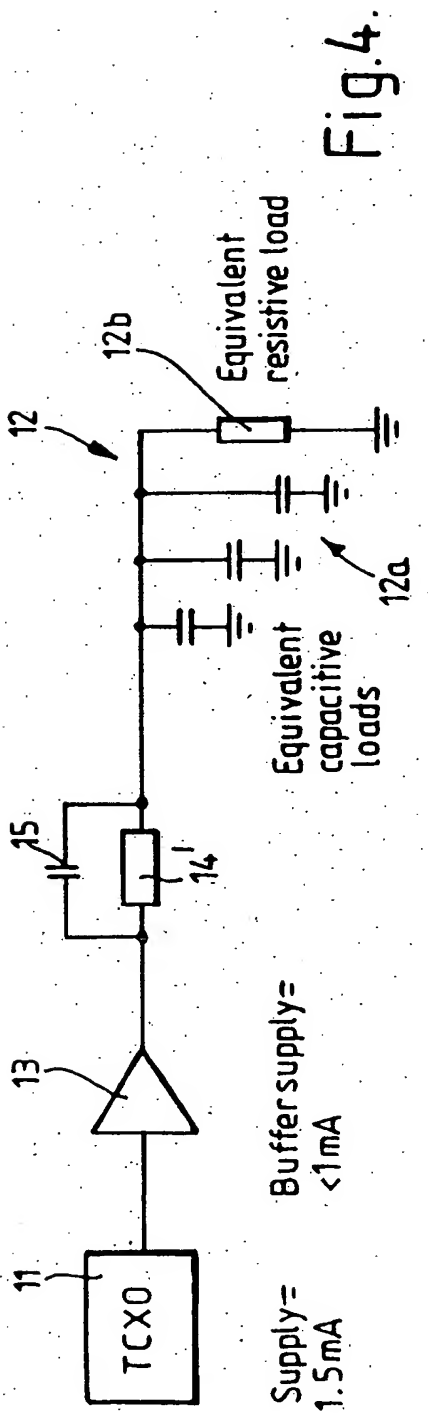
12b
Equivalent resistive load
12
12a
Equivalent capacitive loads
15
14
13
Buffer supply= <1mA
11
TCXO
Supply= 1.5mA

Fig.4.

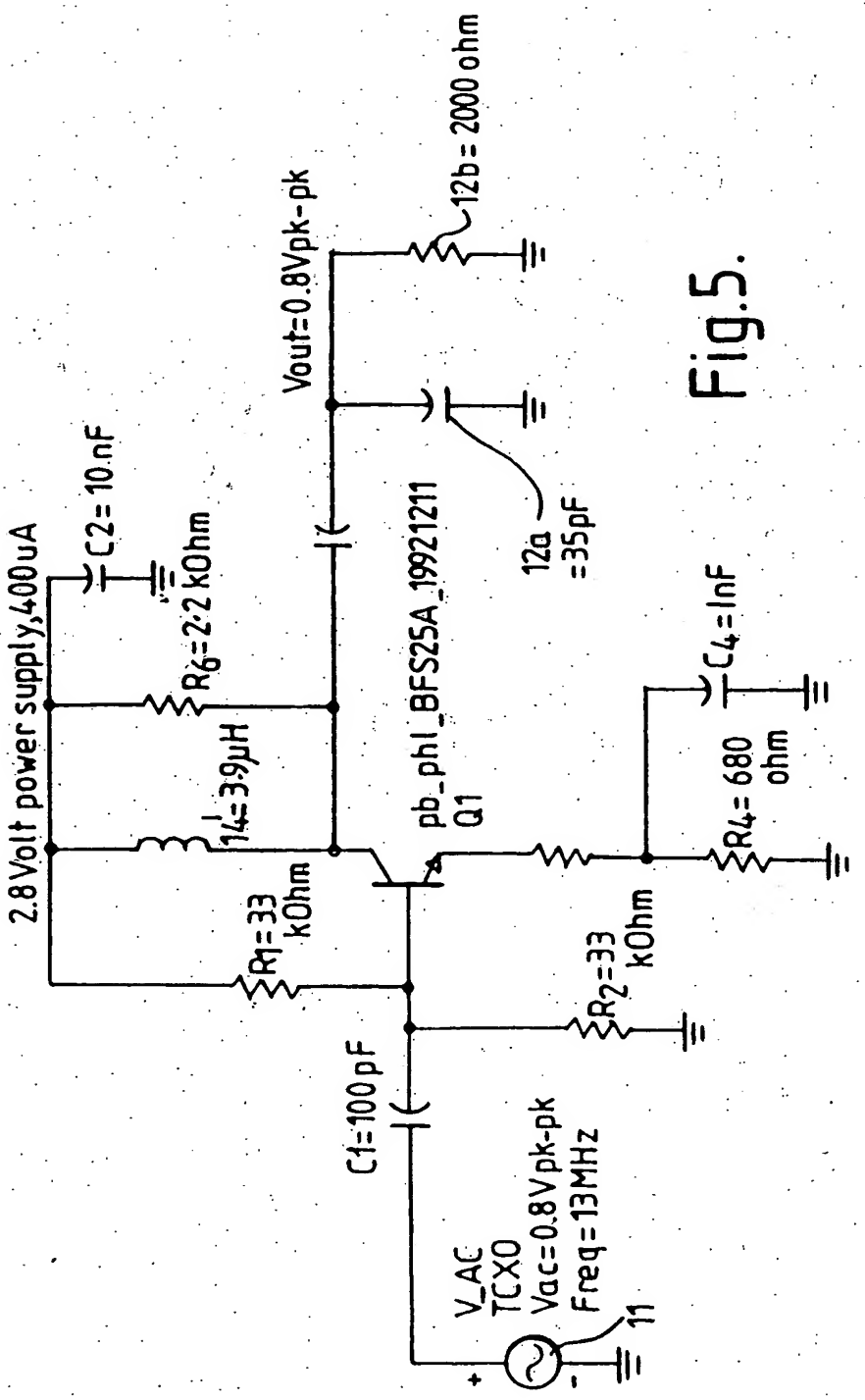
12b= 2000 ohm
Vout=0.8Vpk-pk
C2= 10 nF
12a =35pF
2.8 Volt power supply, 400 uA
R6=2.2 kOhm
C4=1nF
pb_phl_BFS25A_19921211
Q1
14=3.9µH
R4= 680 ohm
R1=33 kOhm
R2=33 kOhm
C1=100 pF
V_AC
TCXO
Vac=0.8Vpk-pk
Freq=13MHz
11

Fig.5.

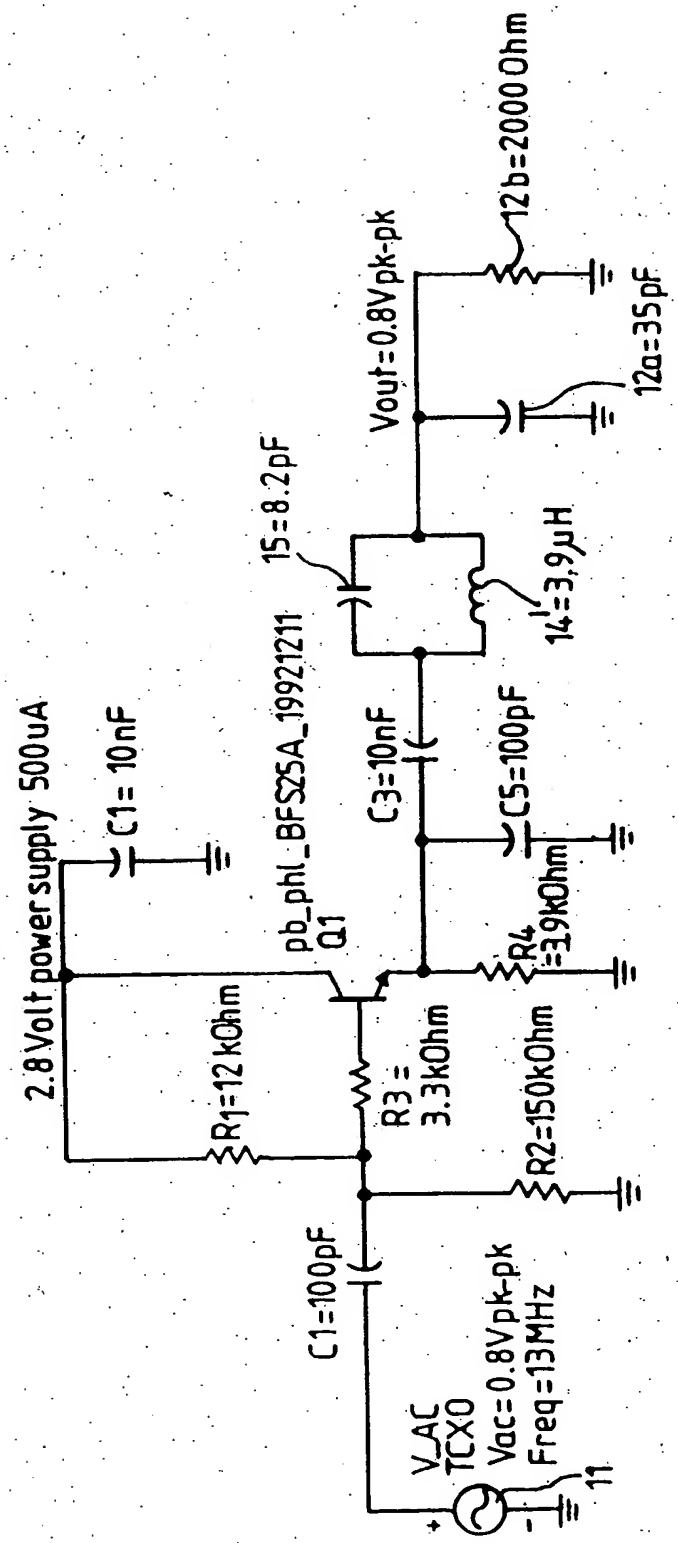
2.8Volt power supply 500uA
C1= 10nF
R1=12 kOhm
pb_phl_BFS25A_19921211
Q1
R3 = 3.3kOhm
R2=150kOhm
C1=100pF
V_AC
TCXO
Vac=0.8Vpk-pk
Freq=13MHz
11
C3=10nF
C5=100pF
R4 =3.9kOhm
15=8.2pF
14=3,9µH
Vout=0.8Vpk-pk
12b=2000 Ohm
12a=35pF

Fig.6.

INTERNATIONAL SEARCH REPORT

International Application No
PCT/GB 02/01324

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G06F1/04

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G06F H03B H03K

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data, IBM-TDB

C. DOCUMENTS CONSIDERED TO BE RELEVANT

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X	US 5 734 285 A (HARVEY GEOFFREY P) 31 March 1998 (1998-03-31) abstract; figures 1-40 column 1, line 20 -column 4, line 49 column 6, line 26, paragraph 35	1-12
X	EP 0 395 146 A (PHILIPS NV) 31 October 1990 (1990-10-31) abstract; figure 1 column 3, line 41 -column 4, line 42	1,2,7,8
A	US 6 204 712 B1 (CAMERLO SERGIO D) 20 March 2001 (2001-03-20) abstract; figure 3 column 5, line 36 - line 57	

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[X] Further documents are listed in the continuation of box C.

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Date of the actual completion of the international search	Date of mailing of the international search report
24 May 2002	05/06/2002

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INTERNATIONAL SEARCH REPORT

International Application No
PCT/GB 02/01324

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	BECKER M E ET AL: "Transmission line clock driver" COMPUTER DESIGN, 1999. (ICCD '99). INTERNATIONAL CONFERENCE ON AUSTIN, TX, USA 10-13 OCT. 1999, LOS ALAMITOS, CA, USA,IEEE COMPUT. SOC, US, 10 October 1999 (1999-10-10), pages 489-490, XP010360531 ISBN: 0-7695-0406-X the whole document	

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/GB 02/01324

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